Claims

1. A method of replacing standard cells with high speed cells in the design of a circuit using a computer program, said application specific integrated circuit design comprising a plurality of high speed cells and a plurality of standard cells, said high speed cells and standard cells being arranged to form a plurality of paths on said application specific integrated circuit, said method comprising the steps of:
timing said plurality of paths
identifying cells occurring on paths for which timing targets are not met;
upgrading at least one of said identified cells to a high speed cell.

2. A method as claimed in claim 1, further comprising the step of determining a first set of paths, wherein said step of identifying cells occurring on paths for which timing targets are not met is performed on paths belonging to the first set of paths.

3. A method according to claim 2 wherein said first set of paths is a set of paths that have the slowest timing.

4. A method according to claim 2 wherein the first set of paths comprises a predetermined number of paths.

5. A method as claimed in claim 2 wherein the first set of paths are ordered according to timing and allocated an order number.

6. A method as claimed in claim 1 wherein the cells identified as occurring on said set of paths for which timing targets are not met are ranked in order of the contribution of the cell to the timing of a path.

7. A method as claimed in claim 6 wherein the contribution of the cell to the timing of the path is calculated using at least one of the
order number of each path the cell occurs on; and
a transition time of the cell.

8. A method as claimed in claim 6 wherein a predetermined number of the highest ranked cells are replaced with high speed cells.

9. A method as claimed in claim 2 wherein the first set of paths comprises paths that begin at one of a plurality of inputs and terminate at one of a plurality of first registers.

10. A method as claimed in claim 2 wherein the first set of paths comprises paths that begin at one of the plurality of first registers and terminate at one of a plurality of second registers.

11. A method as claimed in claim 2 wherein the first set of paths comprises paths that begin at one of the plurality of second registers and terminate at one of a plurality of outputs.

12. A method as claimed in claim 2 wherein the first set of paths are determined from a second set of paths.

13. A method as claimed in claim 1 wherein the application specific integrated circuit design comprises a plurality of end points at which the plurality of paths terminate.

14. A method as claimed in claim 13 wherein the end points are cells.

15. A method as claimed in claim 12 wherein the second set of paths comprises one path per endpoint.

16. A method as claimed in claim 12 wherein the second set of paths comprises a plurality of paths per endpoint.

17. A method as claimed in claim 13 wherein the second set of paths is changed to comprise an increased number of paths per endpoint if the number of paths in the first set of paths is greater than the number of paths for which timing targets are not met.

18. A method as claimed in claim 1 wherein the circuit is an integrated circuit.

19. A method as claimed in claim 18 wherein the integrated circuit is an application specific integrated circuit.

20. A computer program for replacing standard cells with high speed cells in the design of a circuit, said application specific integrated circuit design comprising a plurality of high speed cells and a plurality standard cells, said high speed cells and standard cells being arranged to form a plurality of paths on said application specific integrated circuit, said computer program arranged to carry out the steps of:
timing said plurality of paths;
identifying cells occurring on paths for which timing targets are not met;
upgrading at least one of said identified cells to a high speed cell.

21. A computer program as claimed in claim 20, further arranged to carry out the step of determining a first set of paths, wherein said step of identifying cells occurring on paths for which timing targets are not met is performed on paths belonging to the first set of paths.

22. A computer program according to claim 21 wherein said first set of paths is a set of paths that have the slowest timing.

23. A computer program according to claim 21 wherein the first set of paths comprises a predetermined number of paths.

24. A computer program as claimed in claim 21 wherein the first set of paths are ordered according to timing and allocated an order number.

25. A computer program as claimed in claim 20 wherein the cells identified as occurring on said set of paths for which timing targets are not met are ranked in order of the contribution of the cell to the timing of a path.

26. A computer program as claimed in claim 25 wherein the contribution of the cell to the timing of the path is calculated using at least one of the
order number of each path the cell occurs on; and
a transition time of the cell.

27. A computer as claimed in claim 25 wherein a predetermined number of the highest ranked cells are replaced with high speed cells.

28. A computer program as claimed in claim 21 wherein the first set of paths comprises paths that begin at one of a plurality of inputs and terminate at one of a plurality of first registers.

29. A computer program as claimed in claim 21 wherein the first set of paths comprises paths that begin at one of the plurality of first registers and terminate at one of a plurality of second registers.

30. A computer program as claimed in claim 21 wherein the first set of paths comprises paths that begin at one of the plurality of second registers and terminate at one of a plurality of outputs.

31. A computer program as claimed in claim 21 wherein the first set of paths are determined from a second set of paths.

32. A computer program as claimed in claim 20 wherein the application specific integrated circuit design comprises a plurality of end points at which the plurality of paths terminate.

33. A computer program as claimed in claim 32 wherein the end points are cells.

34. A computer program as claimed in claim 31 wherein the second set of paths comprises one path per endpoint.

35. A computer program as claimed in claim 31 wherein the second set of paths comprises a plurality of paths per endpoint.

36. A computer program as claimed in claim 32 wherein the second set of paths is changed to comprise an increased number of paths per endpoint if the number of paths in the first set of paths is greater than the number of paths for which timing targets are not met.

37. A computer program as claimed in claim 20 wherein the circuit is an integrated circuit.

38. A computer program as claimed in claim 37 wherein the integrated circuit is an application specific integrated circuit.